WHAT IS CLAIMED IS:

1. A multi-port memory system, comprising:

a memory array with an addressable array of memory locations;

at least two ports coupled to the memory array, each of the at least two ports transmitting to the memory array an address, a clock signal, and a read/write control signal; and

a collision detect circuit coupled to receive the address, the clock signal, and the read/write control signal from each of the at least two ports,

wherein the collision detect circuit sets a collision flag when a collision condition is detected in any of the at least two ports.

2. The system of claim 1, further including control logic coupled to the memory array to receive signals associated with the at least two ports and present signals to the memory array.

3. The system of claim 1, wherein the collision detect circuit sets the collision flag associated with one of the at least two ports if another of the at least two ports is executing a write operation to a memory location at the same that that the one of the at least two ports accesses the memory location.

4. The system of claim 1, wherein the collision detect circuit comprises:

an address compare circuit coupled to receive and compare addresses from each of the at least two ports and provide a match signals indicating which of the addresses are the same; and

at least one collision detect logic coupled to receive the match signals and the read/write signals and provide a collision signal for a first port of the at least two ports if the match signals indicate an address match between the first port and a second port of the at least two ports and the read/write signal associated with the second port indicates a write operation; and

at least one collision flag set circuit coupled to receive a collision signal from the collision detect logic and set a collision detect flag according to the clock signal associated with the first port.

5. The system of claim 4, wherein the collision flag set circuit associated with the first port comprises:

a flip-flop circuit that is set according to the collision detect flag;

a first latch that latches an output signal from the flip-flop circuit on a rising edge of the clock signal associated with the first port;

a second latch that latches a signal from the first latch on a falling edge of the clock signal associated with the first port; and

an output driver coupled to receive a signal from the second latch and provide a collision detect flag.

6. The system of claim 5, wherein the flip-flop circuit is reset from the signal from the first latch.

7. The system of claim 5, further including a first-in-first-out circuit to store addresses in response to the collision signal.

8. A dual port memory system, comprising:

a memory array coupled to receive a left port memory address and a right port memory address; and

a collision detect circuit configured to detect a match between the left port memory address and the right port memory address and generate a left port collision flag if the right port is writing data, and generate a right port collision flag if the left port is writing data.

9. The system of claim 8, wherein the collision detect circuit includes

an address compare circuit that provides a match signal when the left port address and the right port address are the same;

a left port collision detect circuit that provides a left port collision signal when the match signal exists and when the right port is writing;

a left port flip-flop that is set on the left port collision signal;

a first left port latch that latches a collision flag from the left port flip-flop on a rising edge of a left port clock signal, wherein the left port flip-flop is reset according to the collision flag output from the first left port latch;

a second left port latch that latches the collision flag from the first left port latch on a falling edge of the left port clock signal; and

a left port output driver that provides the collision flag from the second left port latch.

10. The system of claim 9, further including a flip-flop that stores the left port address according to the left port collision signal.

11. A method of collision detection in a dual port memory system, comprising:

detecting that a left port address to be presented to a left port is identical to a right port address to be presented to a right port; and

generating a left port collision flag if a write operation is being processed for the right port address at the right port.

12. The method of claim 11, further including generating a right port collision flag if a write operation is being processed for the left port address at the left port.

13. The method of claim 12, further including

providing arbitration when either the left port collision flag or the right port collision flag is set.

14. A method of collision detection, comprising:

detecting an address match between two or more ports; and

generating a collision flag for at least one of the two or more ports of any of the other of the two or more ports are writing.

15. A method of collision detection, further comprising:

providing arbitration when the collision flag is set.